RECEIVED
CENTRAL FAX CENTER
MAR 12 2008



**Amendments to the Claims**:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims**:

1. (Original) A method for adaptively minimising the total power consumption of an apparatus comprising a subsystem comprising a mass storage device and a buffer memory, said method comprising the steps of

determining an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate to/from said buffer memory, and

adjusting the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal.

2. (Original) The method according to claim 1, wherein said step of adjusting the buffer size comprises switching on memory banks and/or memory ICs of said buffer memory for increasing the size of said buffer memory, and switching off memory banks and/or memory ICs for decreasing said buffer memory.

3. (Previously presented) The method according to claim 1, wherein the storage device is a harddisk drive and the step of determining an optimum buffer size comprises

determining a harddisk drive data rate,

determining the stream bit-rate to/from the buffer memory, and

determining the optimum buffer size having the lowest power consumption at the determined stream bit-rate.

4. (Original) The method according to claim 3, wherein said optimum buffer size determination step comprises calculating optimum buffer size from a formula, looking up optimum buffer size in a look-up table, or measuring the minimum power consumption of the subsystem in a feedback loop controlling buffer size.

5. (Currently amended) The method according to claim 1, wherein the optimum buffer ~~memory value~~ size is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption, which subsequently is used to determine the optimal buffer size.

6. (Previously presented) The method according to claim 1 comprising powering up extra memory banks and/or memory ICs when a new stream is admitted.

7. (Previously presented) The method according to claim 1, wherein a powering down of a memory bank or IC is either delayed or the buffered data of that memory bank or IC is moved to another memory bank that will remain powered on after which the first bank is shut down immediately, when a stream is stopped and removed.

8. (Previously presented) The method according to claim 1, wherein in case of multiple simultaneous streams, the sum of the bit-rates of all streams is determined.

9. (Original) A circuit for retrieving data from a mass storage device via a memory buffer comprising a processing unit conceived to:

- adaptively activate or deactivate areas of said buffer memory in such a manner that total power consumption of a subsystem comprising said storage device and said buffer memory is minimised for a given streaming rate to/from said buffer memory; and
- retrieve the data from the mass storage device.

10. (Original) An apparatus comprising a subsystem comprising mass storage device, a buffer memory and the circuit according to claim 9.

11. (Original) The apparatus according to claim 10, wherein said buffer memory comprises SDRAM circuits having banks of memory adapted to be independently switched on/off.

12. (Previously presented) The apparatus according to claim 10, wherein a scheduler function executable by the processing unit controls accessing the storage device and the buffer memory.

13. (Original) A computer-readable medium having embodied thereon a computer program for processing by a computer, the computer program comprising code segments for adaptively minimising the total power consumption of a subsystem comprising a mass storage device and a buffer memory, wherein

a first code segment determines an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate from said buffer memory, and

a second code segment adjusts the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal.

14. (New) The method according to claim 2, wherein the storage device is a harddisk drive and the step of determining an optimum buffer size comprises

determining a harddisk drive data rate,

determining the stream bit-rate to/from the buffer memory, and

determining the optimum buffer size having the lowest power consumption at the determined stream bit-rate.

15. (New) The method according to claim 14, wherein the optimum buffer size is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption, which subsequently is used to determine the optimal buffer size.

16. (New) The method according to claim 2, wherein the optimum buffer size is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption, which subsequently is used to determine the optimal buffer size.

17. (New) The method according to claim 3, wherein the optimum buffer size is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption, which subsequently is used to determine the optimal buffer size.

18. (New) The method according to claim 4, wherein the optimum buffer size is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption, which subsequently is used to determine the optimal buffer size.

19. (New) The method according to claim 2, wherein a powering down of a memory bank or IC is either delayed or the buffered data of that memory bank or IC is moved to another memory bank that will remain powered on, after which the first bank is shut down immediately when a stream is stopped and removed.

20. (New) The apparatus according to claim 11, wherein a scheduler function executable by the processing unit controls accessing the storage device and the buffer memory.